WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit comprising: at least one signal amplifying transistor for amplifying an input signal supplied to a gate thereof;

a first bypassing means for bypassing a part of said input signal to a ground side according to the strength of said input signal; and

a second bypassing means for bypassing a part of said input signal to an output side according to the strength of said input signal.

2. A semiconductor integrated circuit as claimed in claim 1,

wherein said first bypassing means includes:

a first bypassing transistor having a drain connected to a bias voltage applying terminal via a resistance and connected to the gate of said signal amplifying transistor via a capacitance, and a gate connected to a first bypass control voltage applying terminal via a resistance; and

a first bias signal strength adjusting resistance having one end connected to a source of said first bypassing transistor, and another end connected to said bias voltage applying terminal via a resistance and grounded via a capacitance.

3. A semiconductor integrated circuit as claimed in claim 2,

wherein said first bypassing transistor is formed by M (M is an integer of 1 or more) transistors connected in series with each other such that a source of a transistor in a preceding stage is connected to a drain of a transistor in a succeeding stage; and

each of the gates of the M transistors is connected to said first bypass control voltage applying terminal via a resistance.

4. A semiconductor integrated circuit as claimed in claim 2,

wherein said second bypassing means includes:

a second bypassing transistor having a drain connected to the drain of said first bypassing transistor, and a gate connected to a second bypass control voltage applying terminal via a resistance; and

a second bias signal strength adjusting resistance having one end connected to a source of said second bypassing transistor, and another end connected to said bias voltage applying terminal via a resistance and connected to a drain of said signal amplifying transistor via a capacitance.

5. A semiconductor integrated circuit as claimed

in claim 4,

wherein said second bypassing transistor is formed by N (N is an integer of 1 or more) transistors connected in series with each other such that a source of a transistor in a preceding stage is connected to a drain of a transistor in a succeeding stage; and

each of the gates of the N transistors is connected to said second bypass control voltage applying terminal via a resistance.

6. A semiconductor integrated circuit as claimed in claim 1, further including a control means for decreasing a drain bias current of said signal amplifying transistor when said first bypassing means bypasses the part of said input signal to the ground side, and interrupting the drain bias current of said signal amplifying transistor when said second bypassing means bypasses the part of said input signal to the output side.

7. A semiconductor integrated circuit as claimed in claim 6,

wherein a source of said signal amplifying transistor is connected to said control means including a transistor; and

a gate of said transistor is connected to a drain bias current control voltage applying terminal via a

resistance.

8. A semiconductor integrated circuit as claimed in claim 6,

wherein a source of said signal amplifying transistor is grounded via a capacitance; and

said control means includes:

a plurality of bias current controlling transistors whose drains are each connected to the source of said signal amplifying transistor and whose gates are connected to a plurality of drain bias current control voltage applying terminals via resistances; and

a plurality of self-bias resistances each having one end connected to one of the sources of said plurality of bias current controlling transistors, and each having another end connected to a reference potential.

9. A semiconductor integrated circuit as claimed in claim 4,

wherein said semiconductor integrated circuit brings said first bypassing transistor and said second bypassing transistor into an OFF state and brings said signal amplifying transistor into an on state when said semiconductor integrated circuit performs a high gain operation.

10. A semiconductor integrated circuit as claimed

in claim 9,

wherein said semiconductor integrated circuit brings said first bypassing transistor into an off state, brings said second bypassing transistor into an ON state, and brings said signal amplifying transistor into an off state when said semiconductor integrated circuit performs a low gain operation.

11. A radio communication apparatus comprising:

an antenna;

an AGC (Auto Gain Control) amplifier for amplifying a signal received by said antenna;

a mixer for mixing an output signal from said AGC amplifier with a predetermined frequency; and

a signal strength detecting circuit for detecting the signal strength of the received signal;

said AGC amplifier including:

at least one signal amplifying transistor for

amplifying an input signal supplied to a gate thereof;

a first bypassing means for bypassing a part of said input signal to a ground side according to the strength of said input signal; and

a second bypassing means for bypassing a part of said input signal to an output side according to the

strength of said input signal.

12. A radio communication apparatus as claimed in claim 11,

wherein said first bypassing means includes:

a first bypassing transistor having a drain connected to a bias voltage applying terminal via a resistance and connected to the gate of said signal amplifying transistor via a capacitance, and a gate connected to a first bypass control voltage applying terminal via a resistance; and

a first bias signal strength adjusting resistance having one end connected to a source of said first bypassing transistor, and another end connected to said bias voltage applying terminal via a resistance and grounded via a capacitance.

13. A radio communication apparatus as claimed in claim 12,

wherein said first bypassing transistor is formed by M (M is an integer of 1 or more) transistors connected in series with each other such that a source of a transistor in a preceding stage is connected to a drain of a transistor in a succeeding stage; and

each of the gates of the M transistors is connected to said first bypass control voltage applying terminal

via a resistance.

14. A radio communication apparatus as claimed in claim 12,

wherein said second bypassing means includes:

a second bypassing transistor having a drain connected to the drain of said first bypassing transistor and a gate connected to a second bypass control voltage applying terminal via a resistance; and

a second bias signal strength adjusting resistance having one end connected to a source of said second bypassing transistor, and another end connected to said bias voltage applying terminal via a resistance and connected to a drain of said signal amplifying transistor via a capacitance.

15. A radio communication apparatus as claimed in claim 14,

wherein said second bypassing transistor is formed by N (N is an integer of 1 or more) transistors connected in series with each other such that a source of a transistor in a preceding stage is connected to a drain of a transistor in a succeeding stage; and

each of the gates of the N transistors is connected to said second bypass control voltage applying terminal via a resistance.

16. A radio communication apparatus as claimed in claim 11, further including a control means for decreasing a drain bias current of said signal amplifying transistor when said first bypassing means bypasses the part of said input signal to the ground side, and interrupting the drain bias current of said signal amplifying transistor when said second bypassing means bypasses the part of said input signal to the output side.

17. A radio communication apparatus as claimed in claim 16,

wherein a source of said signal amplifying transistor is connected to said control means including a transistor; and

a gate of said transistor is connected to a drain bias current control voltage applying terminal via a resistance.

18. A radio communication apparatus as claimed in claim 16,

wherein a source of said signal amplifying transistor is grounded via a capacitance; and

said control means includes:

a plurality of bias current controlling transistors whose drains are each connected to the source of said signal amplifying transistor and whose gates are

connected to a plurality of drain bias current control voltage applying terminals via resistances; and

a plurality of self-bias resistances, each having one end connected to one of the sources of said plurality of bias current controlling transistors, and each having another end connected to a reference potential.

19. A radio communication apparatus as claimed in claim 14,

wherein said AGC amplifier brings said first bypassing transistor and said second bypassing transistor into an OFF state and brings said signal amplifying transistor into an on state when said AGC amplifier performs a high gain operation.

20. A radio communication apparatus as claimed in claim 19,

wherein said AGC amplifier brings said first bypassing transistor into an off state, brings said second bypassing transistor into an ON state, and brings said signal amplifying transistor into an off state when said AGC amplifier performs a low gain operation.